OUR REF AN-C23/2

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MEMORY MAPS FOR VARIOUS PROCESSORS.

Introduction.

A number of customers have expressed an interest in writing software to run on ISBUS systems, and have therefore requested guidelines on the most likely locations that will be adopted as standard for such items as VDU, Keyboard Port, Printer + Tape UARTs etc.
This document offers some comments on memory maps which reconcile a number of conflicting requirements.

Some Definitions.

An addressing space of 4K consecutive addresses, beginning at (hexadecimal) XØØØ is called a 'page', where X is the 'page' number, and may be any one of the 16 digits Ø, 1, 2, 3, 4, 5, 6, 7, 8, 9, A, B, C, D, E, F.
A 64K space which comprises the 16 'pages' defined above is called a 'chapter'.
The 'lesser' ISBUS standard describes a system which uses the A-side 43-way connector, and the 'greater' ISBUS standard describer a system using both A and B sides, ie. 86 ways in all, (minus 2 for the polarising slot A37, B37).
The main features of the 'lesser' and 'greater' ISBUS standards are as follows:-

	'lesser'	'greater'
Memory address lines	ABØ - AB15	ABØ - AB23
Total Memory Addressing space	64K	16M (= 16384K)
ie. no. of 'chapters'	1	256
& no. of 4K 'pages'	16	4096
I/O Address lines	ABØ - AB7	ABØ - AB15
ie. no of I/O 'ports'	256	64K
Data lines	DBØ - DB7	DBØ - DB15

Upgrading:

The 'lesser' allocations have been chosen to suit the popular 8-bit microprocessors such as 6502, 6800, 6802, 6809, 8060, 8080, Z-80 etc., and the 'greater' allocations have been chosen with the newer 16-bit microprocessors in mind (e.g. 8086, 68000, Z8000 etc.)

Care has been taken to try and minimise the problems of upgrading a system as future developments occur, whilst not making 'small' (ie. less than 64K) users pay excessively for features they do not require.

A difficulty that may be encountered for example is that 24-bit memory address decoding is used in the 'greater' system and so all earlier 'lesser' 16-bit addresses will not be fully decoded.

Address Expansion.

The proposed solution is that a NMREQ line only be issued active for the first 'chapter' of 16 'pages', i.e. for the first 64K addresses. A new NEMREQ line ('Extended' memory request) is allocated for the remaining 255 'chapters', each one of which is a further 64K.

In this way existing cards will not 'crash' into the expanded addresses since the expanded addresses will be accompanied by the absence of the NMREQ line.

I/O Port Expansion.

The 'lesser' standard suits 256 I/O ports, and the 'greater' standard suits 64K of I/O ports. The potential conflict, where the two spaces entirely overlap, is prevented by issuing NI/OREQ only with the first 256 addresses, and a new signal NEI/O REQ (extended I/O request) with the remainder, just as for the address expansion described above.

This memory and I/O expansion technique will require some extra circuitry on the CPU cards so that they can present the appropriate output signals to the bus.
CPU cards designed by Greenbank Electronics will provide these signals, but existing cards from other manufacturers do not do so at present. (The matter is academic for those cards which provide for no connections to the B side of the edge connector, since they can only be used in 'lesser' (<64K) systems anyway).

Design for I/O boards.

It is suggested that designers of cards which use I/O ports adopt a full 16-bit address decoder, and use double sided connectors, to make their cards more suitable for use in the 'greater' systems. They may of course simply use the first 256 ports with NI/OREQ in which case only 8 address bits need be decoded for each, but this actively prevents their use for the 64K or so ports defined for the 'greater' system.

Data Bus Expansion.

As 16-bit data buses take over from 8-bits, new memory cards etc. will have to be 16-data bits wide if they are not to be used in pairs. For the moment 8-bits of data will be sufficient, since such cards can easily be used in a 16-bit system, by adding another 'upper 8-bit' card at the same address. This possibility has been allowed for in the design of the RRM-14 card from Greenbank Electronics - a double sided connector has been provided, and the tracks laid out so that the upper 8 data lines DB8-DB15 can be used instead of the normal lower 8 DBØ-DB7.

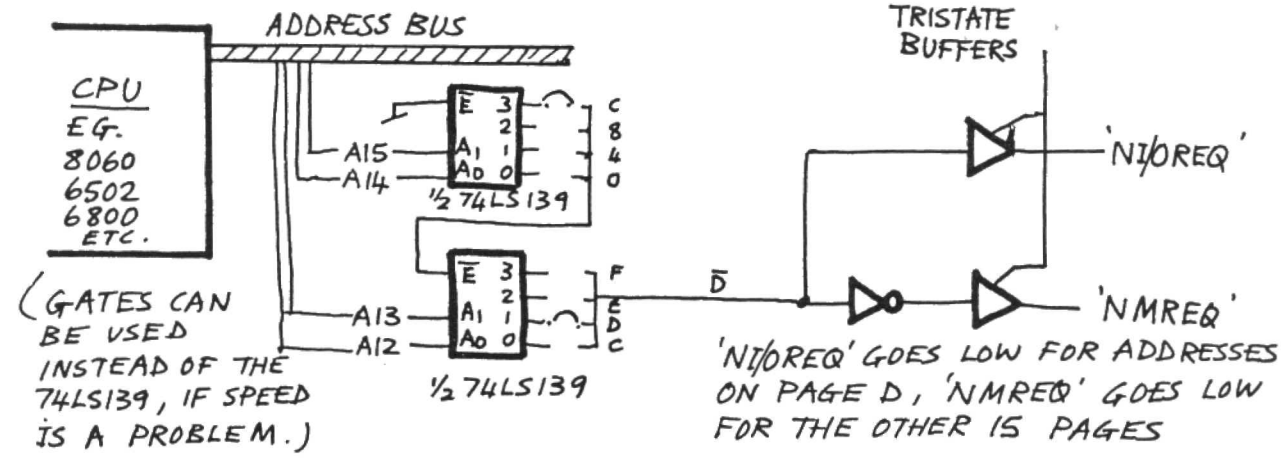
I/O Arrangements for 'Lesser' Systems with I/O-lacking CPUs.

Some microprocessors e.g. INS 8060, 6502, 6800 etc. do not issue a separate I/O address, and therefore all I/O has to be memory-mapped. It will never be possible to directly address the 64K of I/O ports used in the 'greater' systems (since this would leave no addresses for memory!), but it is fairly easy to make these CPUs mimic the effect of the NMREQ and NIOREQ lines issued by for example the Z-80. The design of the CPU card needs to be such that 256 or more addresses are removed from the memory map and diverted to I/O use. Our own suggestion is that the whole of page 'D' be used; this does waste a whole 4K on a mere 256 ports, but it makes for a fairly quick and simple 'retrofit' on any existing boards that may still be in use.

Why Page 'D'?

It might be argued that a page such as 'E' or 'F' would be better for an untidy activity such as this, but 'E' and 'F' are often used for firmware in many competing systems, and we would not wish to prohibit our customers from buying from someone else. (Examples of firmware available are monitor programs for 6502 e.g. 'Tangerine': 'Apple' or 8K BASIC for Z-80 e.g 'Nascom').

Circuit to give I/O on page 'D'



It is assumed that the modification to page D I/O has been carried out to achieve the memory maps presented below.

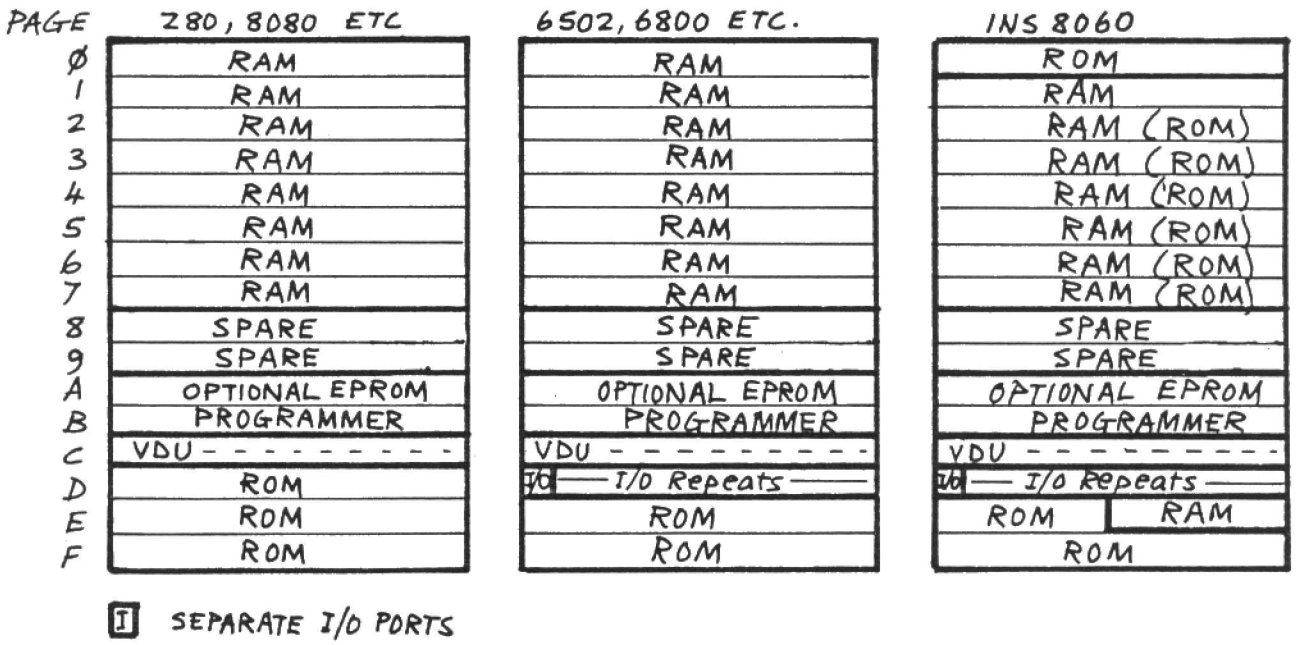
Memory Maps for the 'lesser' (64K) systems with 3 families of MPU

The 3 classes of microprocessor (MPU) considered here are as follows:

① ROM or RAM at Ø, separate I/O ports: e.g. Z80, 8080

② ROM on page F, no separate I/O addresses: e.g. 6502, 6800 6802 etc.

③ ROM on page Ø, no separate I/O addresses: e.g. INS 8060. (An additional requirement that monitor programs for the INS-8060 (SC/MP) generally have is the necessity for both ROM and RAM to be present on the same 4K page, and this fact is allowed for in the memory map suggested).



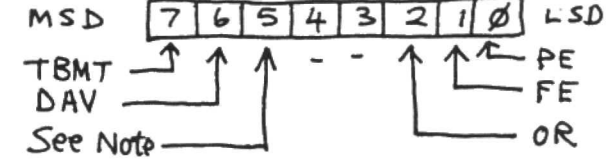
Some suggestions of possible uses for the address are given on the following pages. Since these notes are intended as a guide to potential authors of suitable software, not all the software mentioned is yet available.

① Z80, 8080 etc.

Address	Use
ØØØØ - Ø7FF	2K Machine code monitor (or larger CP/M Disk operating system running in RAM)
ØFFF growing down to Ø8ØØ	Monitor stack and RAM for machine code work.
1ØØØ growing up to 7FFF	28 K RAM (BASIC's stack, text etc.)
8ØØØ - 9FFF	Spare 8K
AØØØ - AFFF	1K/2K/4K space for empty 2508/2516/2532, ie. the EPROM to be programmed.
BØØØ - BFFF	1K/2K/4K space for 'master' or 'source' EPROM which is used to make copy EPROMs (Note: If future expansion means that the 8K EPROM type 2564 is to be programmed then it is suggested this covers the whole space AØØØ - BFFF, and some other location be found for a 'master' or 'source' EPROM if one is required.)
CØØØ growing up to CFFF	Memory-mapped VDU, up to a maximum of 4K.
DØØØ - D7FF	Machine code monitor, source firmware (is copied into RAM at ØØØØ and run there).
D8Ø Ø - DFFF	Further firmware expansion.
EØØØ - FFFF	2K/8K BASIC if available (2K BASIC should include 'power on jump' facilities so that it can be used with the MZB-3 Kemitron board, even mounted on the MZB-3 board in a minimum system).
XØØØ (to be defined)	Boot PROM start address. This overlays the memory map at reset to boot in the CP/M disk operating system. (But note the only version of CP/M available from Kemitron does not use a memory mapped VDU, Keyboard etc.).

Port no. ØØ

Terminal UART Status Byte :



Note: bit number 5 may be used to gate the status of a front panel switch onto the data bus to be read. This could be used for example with the following significance: '1' (or card absent) = 'Terminal not present'
'Ø' = 'Terminal present'.
(Such a switch may or may not be optional).

Port no. Ø1 — Terminal UART Data Byte: 8-bit true data.

Port no. Ø2 — Printer 1 UART Status Byte:
This has bits with the same significance as described for the Status Byte at Port no. ØØ (above).
ie. switch at '1' (or card absent) = 'Do not print'
—"— 'Ø' = 'Print required'

(If the 'Kemitron' SIO-2 board is used there is a facility on the higher numbered status port of each pair to accept a printer 'busy' signal, and force a 'Ø' on to the TBMT Status bit, which then has a dual significance: '1' = transmit buffer empty and printer not busy)

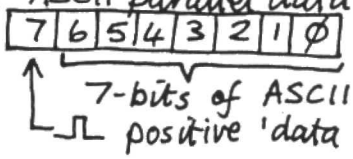
Port no. Ø3 — Printer 1 UART Data Byte: 8-bit true data.

Port no. Ø4 — Tape UART Status: (similar to port ØØ in function)
—"— Ø5 — Tape UART Data: (similar to port Ø1 in function)

Port no. Ø6 — Printer 2 UART Status: (similar to port Ø2 in function)
—"— Ø7 — Printer 2 UART Data: (similar to port Ø3 in function).

Note on Printers: If only one printer is available it will be used in Printer 1 or Printer 2 position. Usually Printer 1 will accompany the Terminal Ports ØØ, Ø1 (ie. in Floppy Disk systems) and Printer 2 will accompany the Tape Ports Ø4, Ø5 (ie. in 'home' computers with cassette tape). Note also that data is normally only sent to the Printer Ports, it is not expected that they will have data available, therefore the DAV etc. bits have a 'don't care' significance.

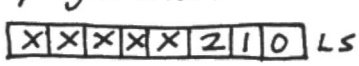
Port no. 4Ø — Keyboard ASCII parallel data + strobe:



Ports. 7Ø – 8F — Reserved for single + double sided disk controller (not always all used).

Port Nos. CØ-CF — Output Ports for e.g. Sound Effects for Space Games.

Port No. FØ — Control word for optional 1K/2K/4K EPROM programmer:



0 : Power on/off
1 : 25 V on/off
2 : Programming Pulse On/Off
X : Don't Care

} for 2508, 2516, 2532 (2708's are slightly different)

Port No. FF — Boot PROM control port:
- Read from port FF = restore addresses after power on jump completed.
- Write to port FF = disable Boot PROM (which has previously been overlaying the memory map after power on jump).

② 6502, 6800, 6802 etc.

Address	Use
ØØØØ growing up to ØFFF	Machine code monitor RAM stack, scratchpad + working area.
1ØØØ growing up to 7FFF	28K RAM (BASIC's stack, text etc.)
8ØØØ – CFFF	As described for Z-80 etc. system - see sheet 6.
DØØØ – DØFF and repeats	I/O 'Ports' in the memory space, each as defined for Z-80 etc system, - see sheet 6, but with the prefix 'DØ' to each port number e.g keyboard port ØØ now DØØØ
EØØØ – FFFF	8K BASIC firmware (if available), including start up vectors etc at FFFF down

③ INS 8060

Address	Use
ØØØØ – ØFFF	NIBL BASIC Interpreter (Part)
1ØØØ – 7FFF	NIBL RAM (Stack, text etc.) Addresses 2ØØØ - 7FFF may optionally be ROM, 2ØØØ is NIBL's 'start up' page for ROM.
8ØØØ – DFFF	As for 6502 etc system described above.
EØØØ – E7FF	Machine code monitor, and remaining part of NIBL BASIC Interpreter.
EFFF growing down to E8ØØ	Monitor stack and machine code RAM area.
FØØØ – FFFF	Further firmware expansion.

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